CLAIMS

What is claimed is:

1. An integrated circuit structure comprising:

a capacitor having metal plates separated by an insulator; and

a semiconductor transistor electrically connected to said capacitor and having a metal gate.

2. The integrated circuit structure in claim 1, wherein said metal gate and one of said metal plates comprise the same metal level in said integrated circuit structure.

3. The integrated circuit structure in claim 1, wherein said capacitor comprises a vertical capacitor having an upper metal plate vertically over a lower metal plate.

4. The integrated circuit structure in claim 3, wherein said metal gate and said upper metal plate comprise the same metal level in said integrated circuit structure.

5. The integrated circuit structure in claim 3, wherein said transistor includes a drain region connected to lower metal plate.

6. An integrated circuit structure comprising:

a pair of capacitors, each having metal plates separated by an insulator; and

semiconductor transistors, each being electrically connected to one of said capacitors, wherein each of said semiconductor transistors has a metal gate.

7. The integrated circuit structure in claim 6, wherein each said metal gate of said transistors and one of said metal plates of each of said capacitors comprise the same metal level in said integrated circuit structure.

8. The integrated circuit structure in claim 6, wherein each of said capacitors comprise a vertical capacitor having an upper metal plate vertically over a lower metal plate.

9. The integrated circuit structure in claim 8, wherein each said metal gate of said transistors and each said upper metal plate of said capacitors comprise the same metal level in said integrated circuit structure.

10. The integrated circuit structure in claim 8, wherein each of said transistors includes a drain region connected to a respective lower metal plate of an adjacent capacitor.

11. A method of forming a metal-insulator-metal capacitor and an associated semiconductor transistor having a metal gate, said method comprising:

forming a first metal layer;

forming an insulator over said first metal layer;

removing a portion of said first metal layer from a gate region; and

forming a second metal layer over said insulator and in said gate region,

wherein said second metal layer comprises a gate of said transistor and a plate of said transistor.

12. The method in claim 11, further comprising forming sidewall spacers adjacent sacrificial gate structures, wherein said first metal layer is formed over said sidewall spacers.

13. The method in claim 11, further comprising, after said forming of said sidewall spacers, doping source and drain regions in said substrate.

14. The method in claim 11, further comprising planarizing said first metal layer.

15. The method in claim 14, wherein said planarizing of said first metal layer reduces voids and surface irregularities in said second metal layer.

16. The method in claim 11, further comprising forming an insulator over said first metal layer.

17. The method in claim 16, wherein said insulator comprises both a capacitor insulator and a gate insulator.

18. The method in claim 11, wherein said plate comprises an upper plate of said capacitor.

19. A method of forming a metal-insulator-metal capacitor and an associated semiconductor transistor having a metal gate, said method comprising:

patterning sacrificial gate structures over a substrate;

forming sidewall spacers adjacent said sacrificial gate structures;

forming a first metal layer adjacent said sidewall spacers;

planarizing said first metal layer;

removing said sacrificial gate structures;

forming an insulator over said first metal layer;

removing a portion of said first metal layer from a gate region; and

forming a second metal layer over said insulator and in said gate region,

wherein said second metal layer comprises a gate of said transistor and a plate of said transistor.

20. The method in claim 19, wherein said planarizing of said first metal layer reduces voids and surface irregularities in said second metal layer.

21. The method in claim 19, wherein said insulator comprises both a capacitor insulator and a gate insulator.

22. The method in claim 19, further comprising, after said forming of said sidewall spacers, doping source and drain regions in said substrate.

23. The method in claim 21, wherein said plate comprises an upper plate of said capacitor.